IN THE CLAIMS:

Claims 1-40 (Canceled)

41. (Previously Presented) A semiconductor device, comprising:

a co-doped germanium buried layer located over a doped substrate;

a doped epitaxial layer located over said co-doped germanium buried layer

a gate structure located over said doped epitaxial layer, said gate structure including a gate dielectric and gate electrode; and

source/drain regions located within said doped epitaxial layer proximate said gate structure, wherein said source/drain regions do not extend into said co-doped germanium buried layer.

42. (Previously Presented) The semiconductor device as recited in Claim 41 wherein said co-doped germanium buried layer includes a p-type dopant.

43. (Previously Presented) The semiconductor device as recited in Claim 42 wherein said p-type dopant is boron.

44. (Previously Presented) The semiconductor device as recited in Claim 41 wherein said co-doped germanium buried layer has a germanium concentration ranging from about 2E20 atoms/cm^3 to about 7E20 atoms/cm^3.

45. (Previously Presented) The semiconductor device as recited in Claim 41 wherein said co-doped germanium buried layer has a thickness ranging from about 1 μm to about 10 μm.

46. (Previously Presented) The semiconductor device as recited in Claim 41 wherein said doped substrate, said co-doped germanium buried layer, and said epitaxial layer collectively have a thickness ranging from about 2 μm to about 20 μm.

47. (Previously Presented) The semiconductor device as recited in Claim 41 wherein a first doped lattice matching layer is located between said doped substrate and said co-doped germanium buried layer and a second doped lattice matching layer is located between said co-doped germanium buried layer and said doped epitaxial layer.

48. (Previously Presented) The semiconductor device as recited in Claim 47 wherein dopant concentrations of said first and second doped lattice matching layers are each less than a dopant concentration of said co-doped germanium buried layer.

49. (Previously Presented) The semiconductor device as recited in Claim 48 wherein a dopant concentration of said doped substrate is less than said dopant concentration of said first doped lattice matching layer and a dopant concentration of said doped epitaxial layer is less than said dopant concentration of said second doped lattice matching layer.

50. (Previously Presented) The semiconductor device as recited in Claim 48 further including a third doped lattice matching layer located between said first doped lattice matching layer and said co-doped germanium buried layer and a fourth doped lattice matching layer located between said second doped lattice matching layer and said co-doped germanium buried layer.

51. (Previously Presented) The semiconductor device as recited in Claim 50 wherein a dopant concentration of said third doped lattice matching layer is more than said dopant concentration of said first doped lattice matching layer and a dopant concentration of said fourth doped lattice matching layer is more than said dopant concentration of said second doped lattice matching layer.

52. (Previously Presented) The semiconductor device as recited in Claim 47 wherein said first and second doped lattice matching layers each include a dopant gradient wherein a dopant concentration of each of said dopant gradients is greater adjacent said co-doped germanium buried layer.

53. (Previously Presented) The semiconductor device as recited in Claim 41, further including interconnects located within interlevel dielectric layers for contacting said transistor.